

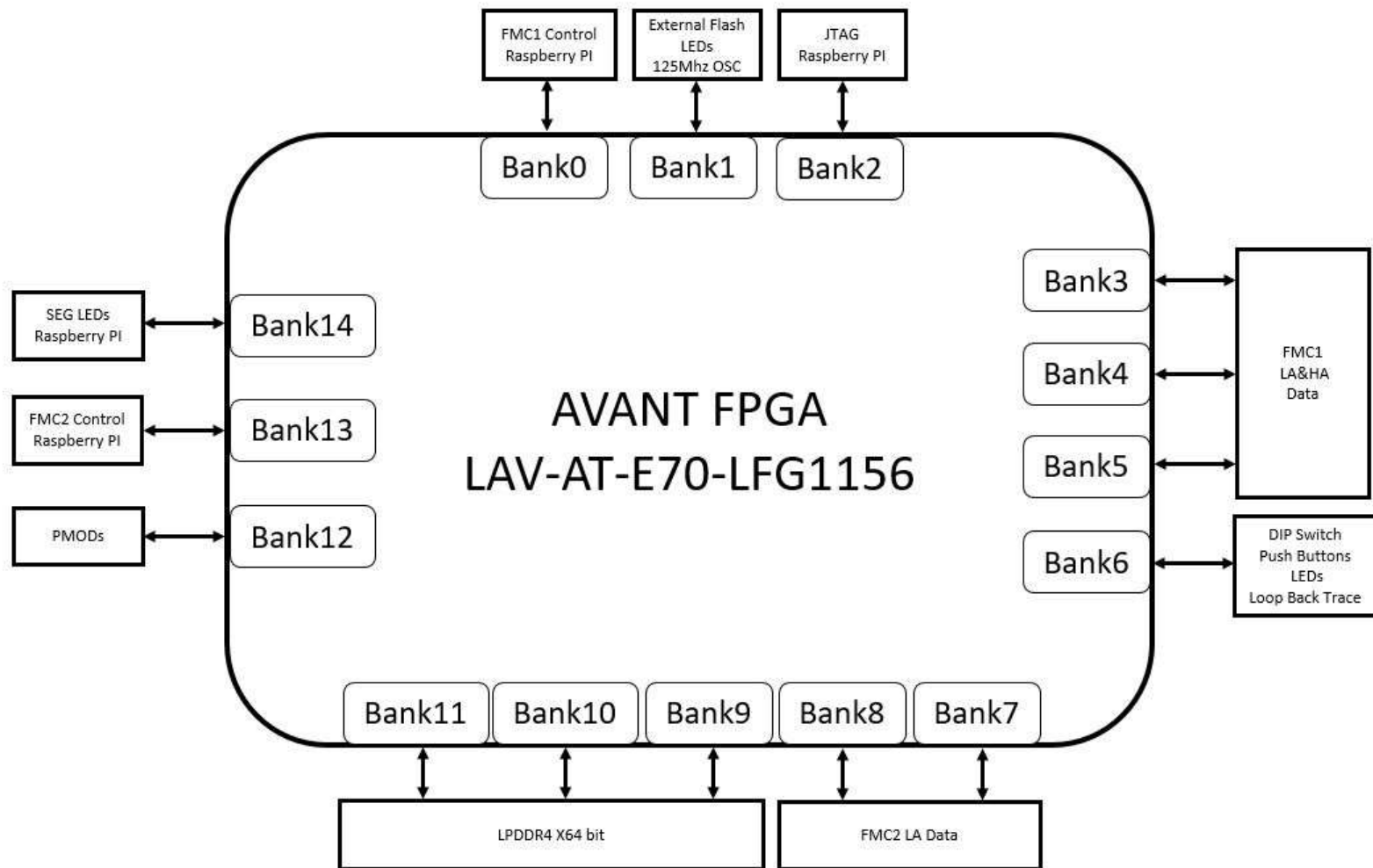
Avant-E70 Development Board REVA

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- 02 - Block Diagram
- 03 - USB Interface
- 04 - Bank-0,1 External Flash
- 05 - Bank-2 JTAG, UART
- 06 - Bank-3,4,5 FMC1
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- 21 - Power Block Diagram



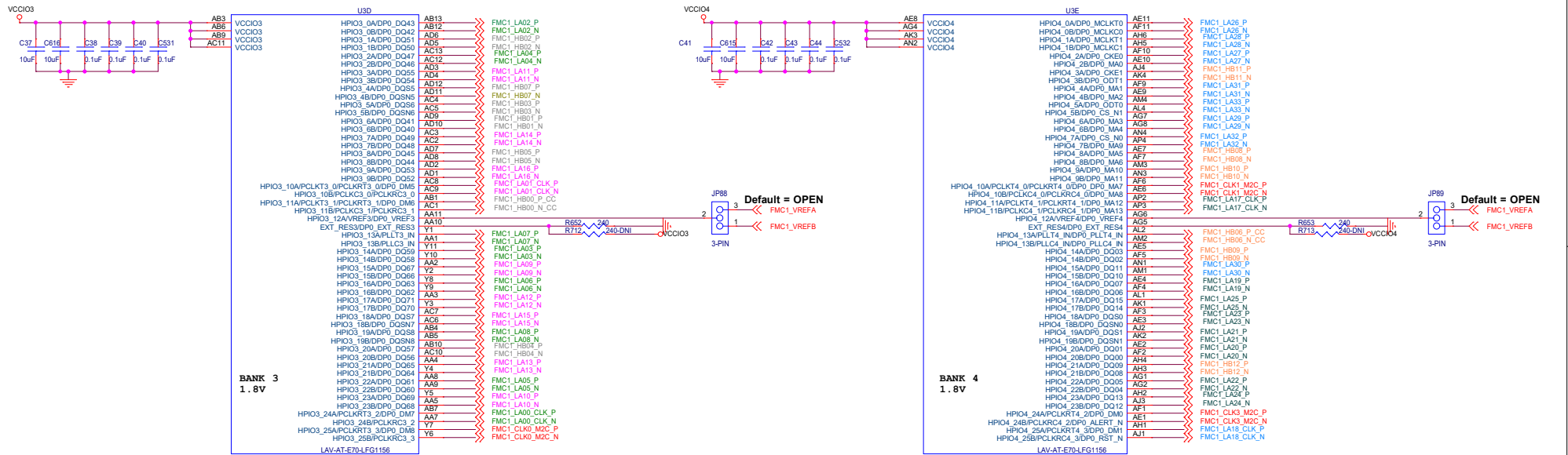
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Title			Title Page		
Size	Project			Schematic Rev 1.0	
	B Avant-E70 Development Board			Board Rev A	
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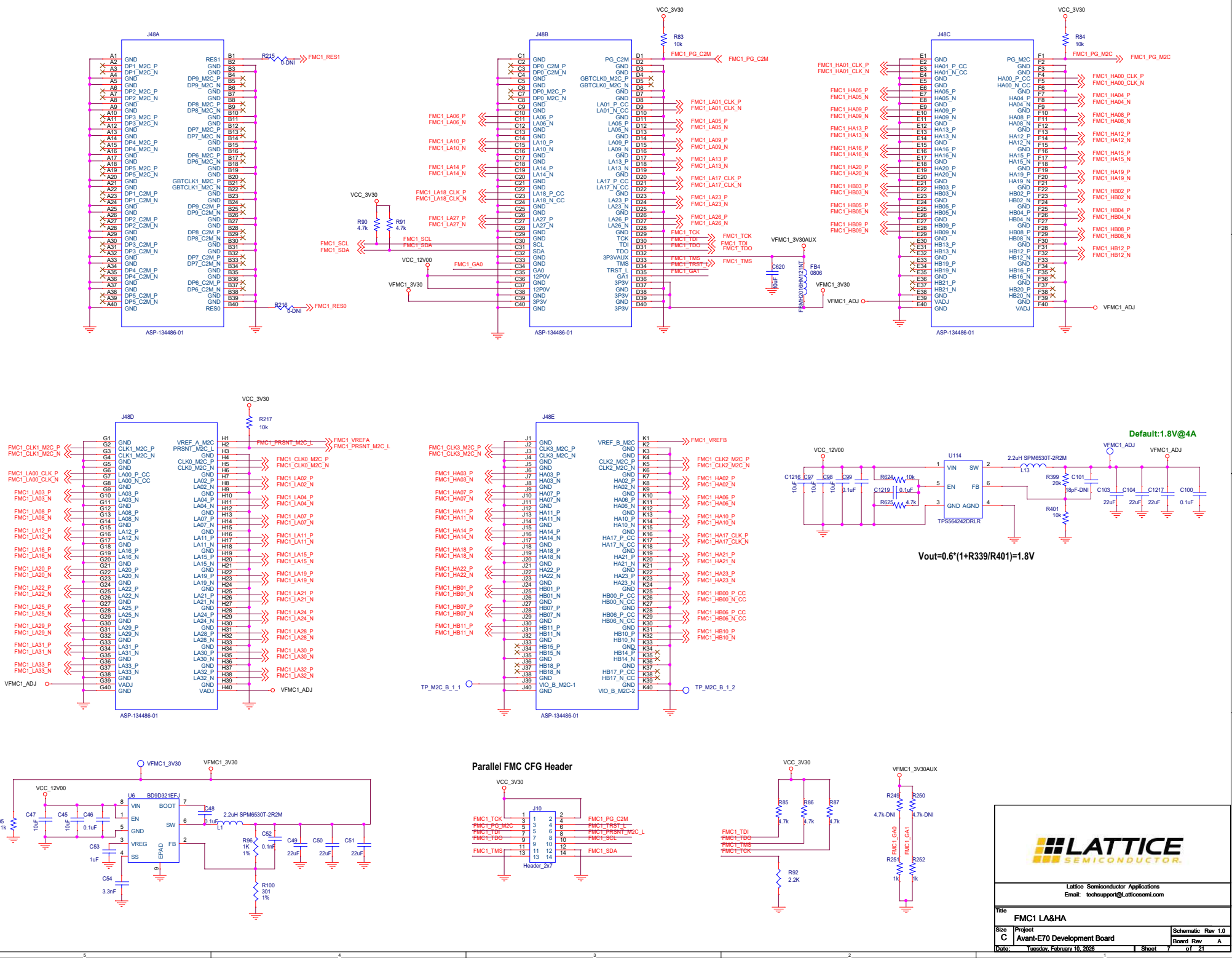
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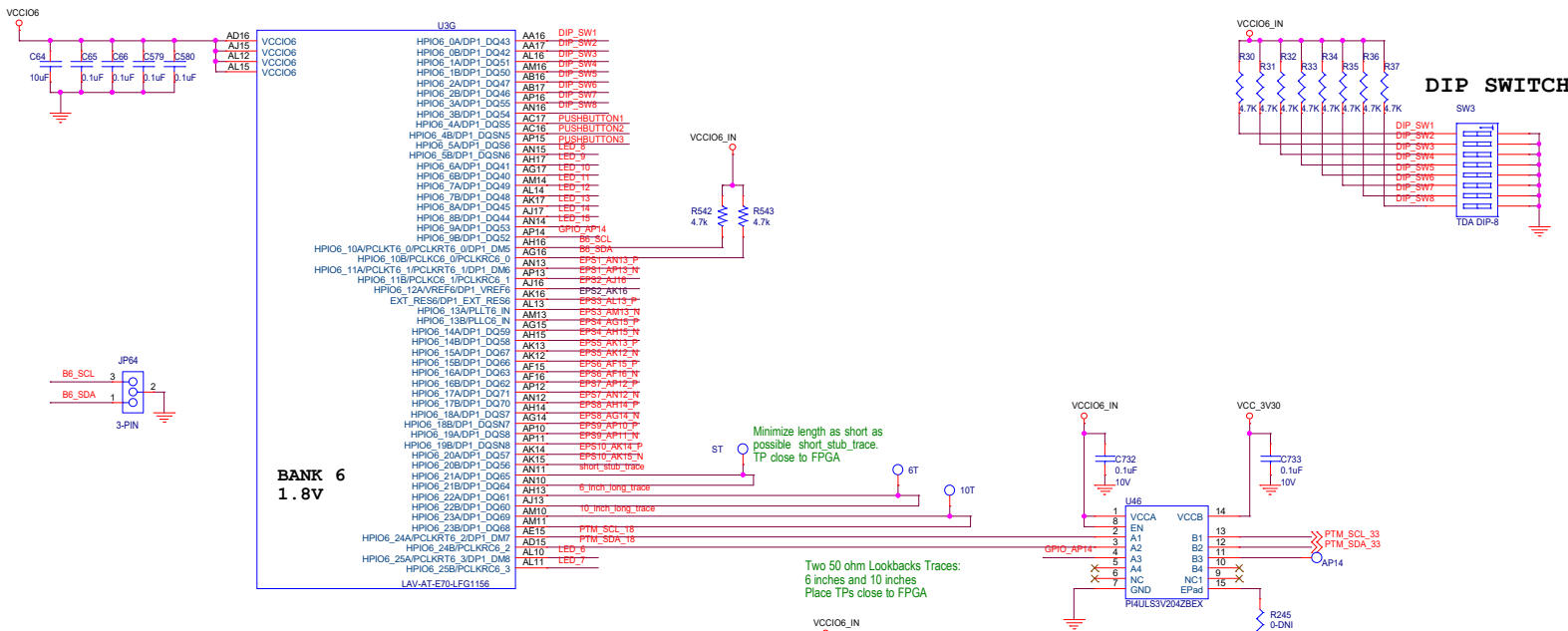
Title			Block Diagram
Size	Project		Schematic Rev 1.0
	Avant-E70 Development Board		Board Rev A
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Title Bank 3,4,5 FMC1			
Size C	Project Avant-E70 Development Board	Schematic Rev 1.0	
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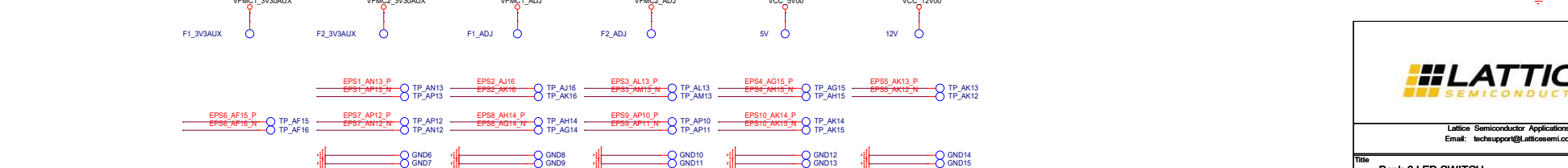
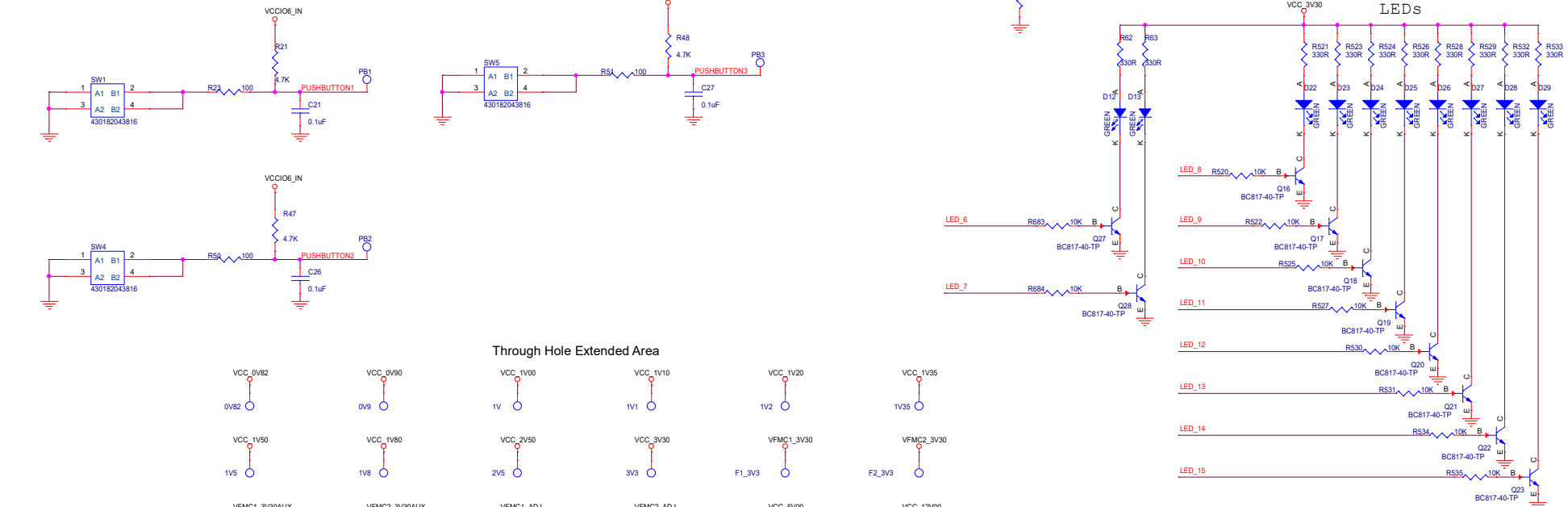


Switch Signal Map

U3 pin	Signal	SWITCH
AA16	DIP_SW1	1
AA17	DIP_SW2	2
AL16	DIP_SW3	3
AM16	DIP_SW4	4
AB16	DIP_SW5	5
AB17	DIP_SW6	6
AP16	DIP_SW7	7
AN16	DIP_SW8	8

LEDs Signal Map

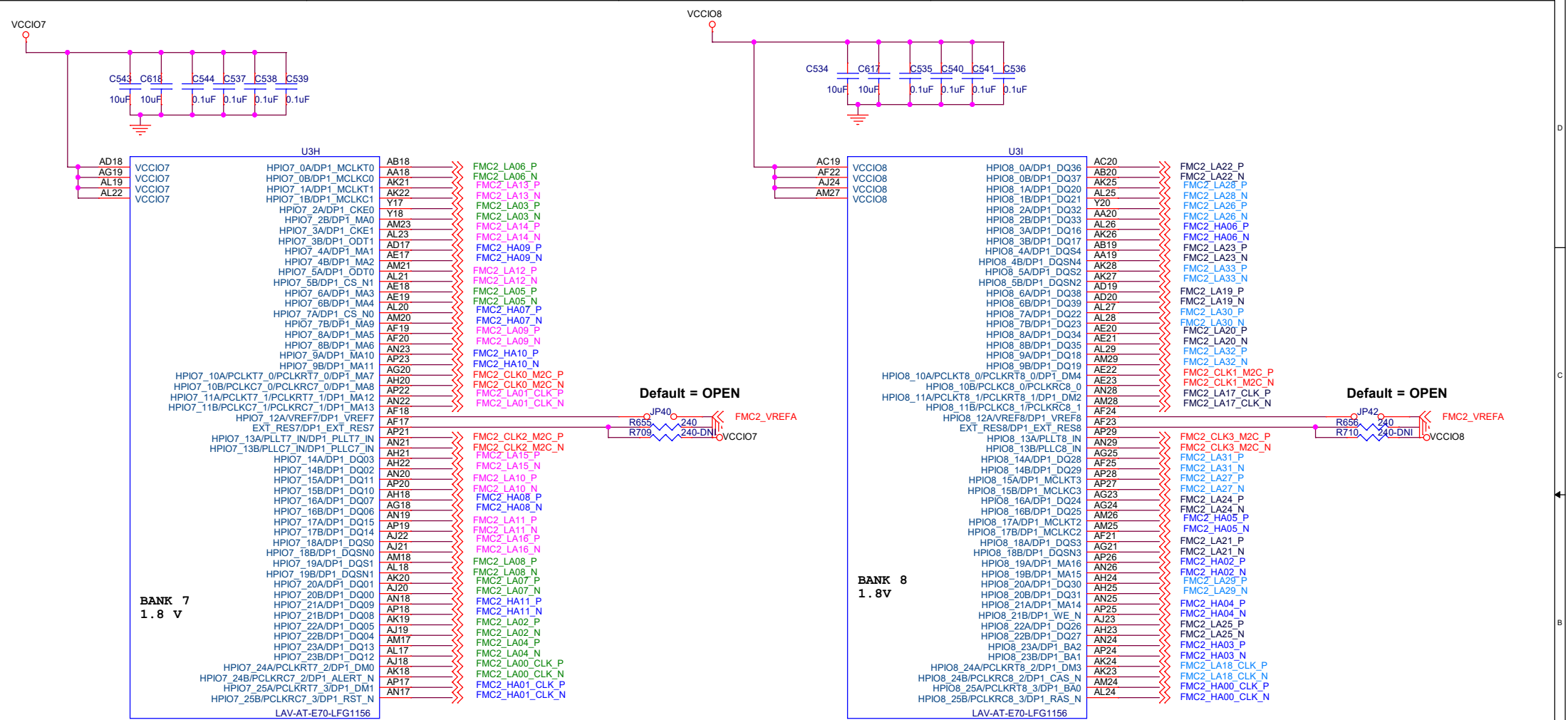
U3 pin	Signal	LED
AL10	LED_6	D12
AL11	LED_7	D13
AN15	LED_8	D22
AH17	LED_9	D23
AG17	LED_10	D24
AM14	LED_11	D25
AL14	LED_12	D26
AK17	LED_13	D27
AJ17	LED_14	D28
AN14	LED_15	D29



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Title Bank-6 LED, SWITCH		
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LVCMOS&LVDS Through Hole Extended Area



FMC2 Supported:
LA[0:33]
HA[0:11]

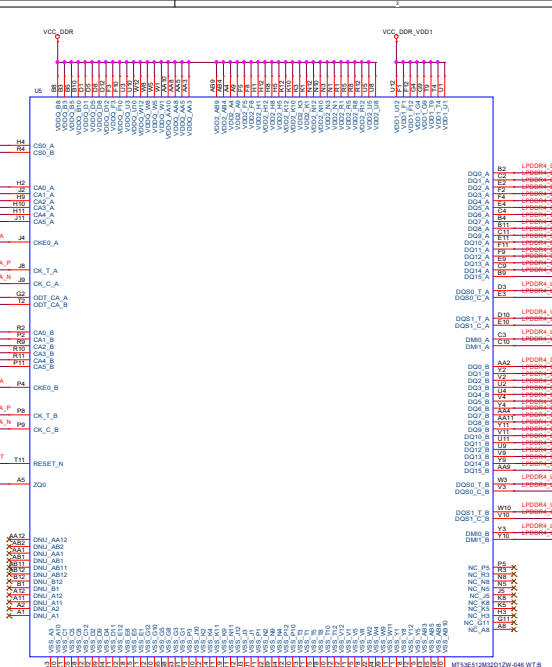
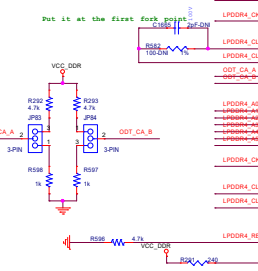


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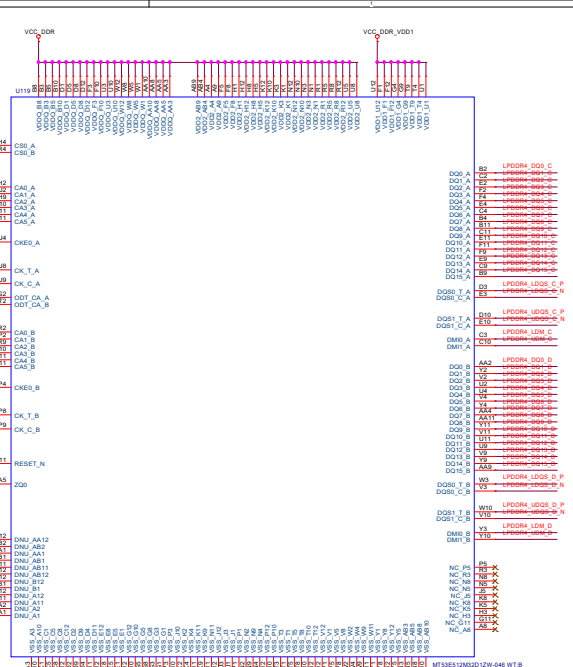
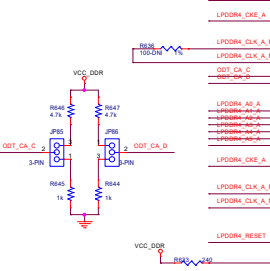
Title			Bank-7,8 FMC2	
Size	Project	Avant-E70 Development Board		Schematic Rev 1.0
	B			Board Rev A
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DDR Layout notice: T-branch topology for CLK and CA bus

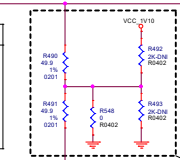


DDR Layout notice: T-branch topology for CLK and CA bus

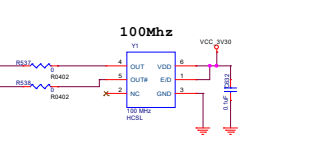


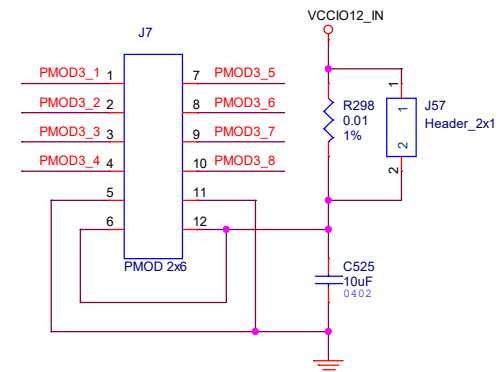
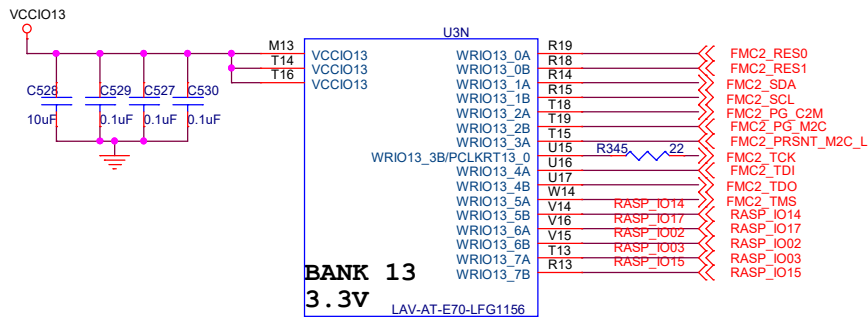
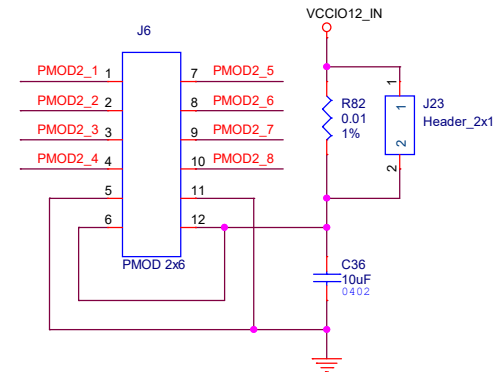
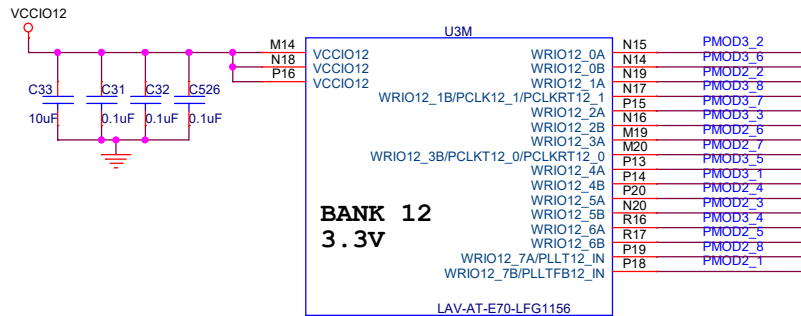
	HCSL (Default)	LVDS
R490	49.9 Ohms	49.9 Ohms
R491	49.9 Ohms	49.9 Ohms
R492	DNP	2K Ohms
R493	DNP	2K Ohms
R537	0 Ohm	0.1 uF
R538	0 Ohm	0.1 uF
R548	0 Ohm	0.1 uF

Place R490, R491 & R548 close to FPGA



Place this termination circuit to back side of board close to FPGA (not close to Y1)

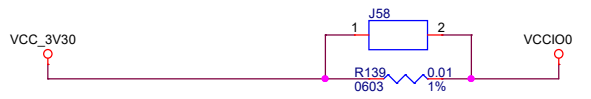




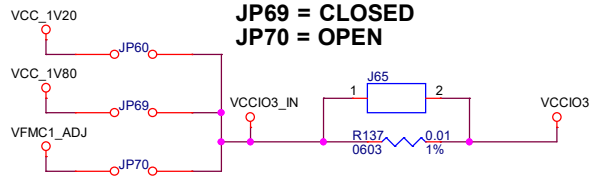
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Title			Bank-12,13 PMODs	
Size	Project		Schematic Rev 1.0	
	Avant-E70 Development Board		Board Rev A	
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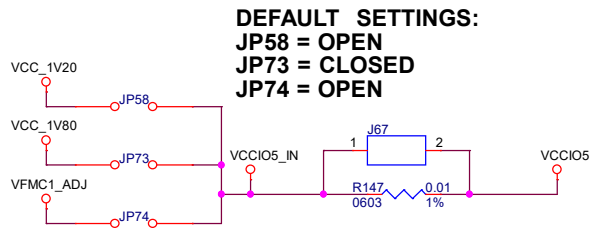
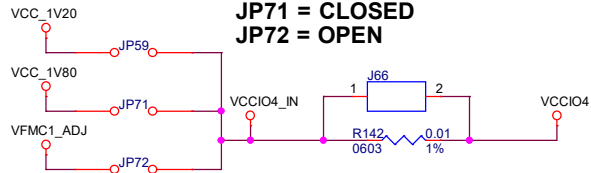
Title			
Bank-14 Segment & RPi			
Size B	Project Avant-E70 Development Board	Schematic Rev 1.0	
		Board Rev	A
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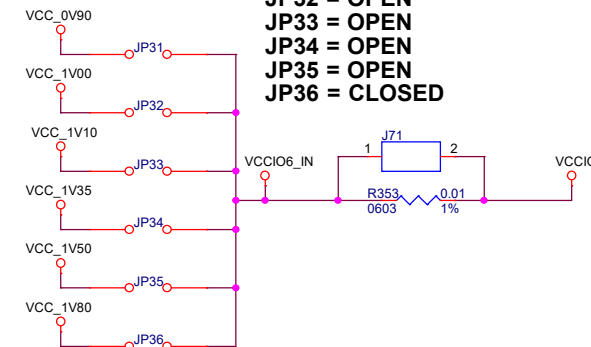
DEFAULT SETTINGS:
JP60 = OPEN
JP69 = CLOSED
JP70 = OPEN



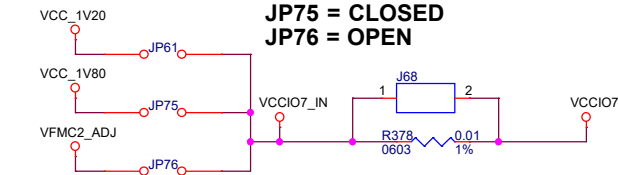
DEFAULT SETTINGS:
JP59 = OPEN
JP71 = CLOSED
JP72 = OPEN



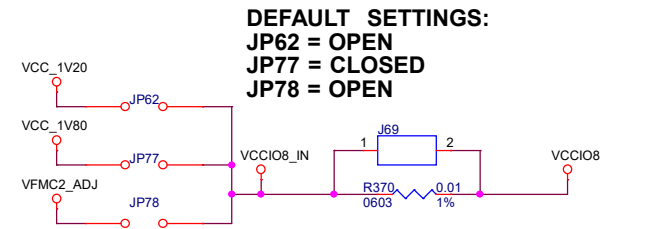
DEFAULT SETTINGS:
JP58 = OPEN
JP73 = CLOSED
JP74 = OPEN



DEFAULT SETTINGS:
JP31 = OPEN
JP32 = OPEN
JP33 = OPEN
JP34 = OPEN
JP35 = OPEN
JP36 = CLOSED



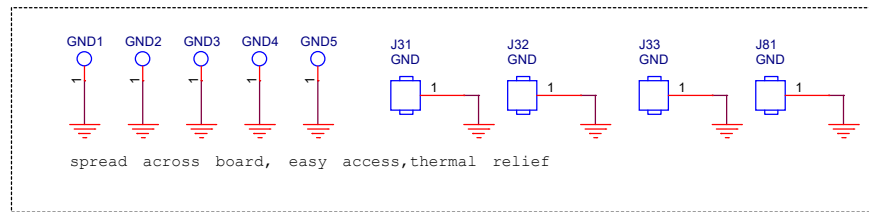
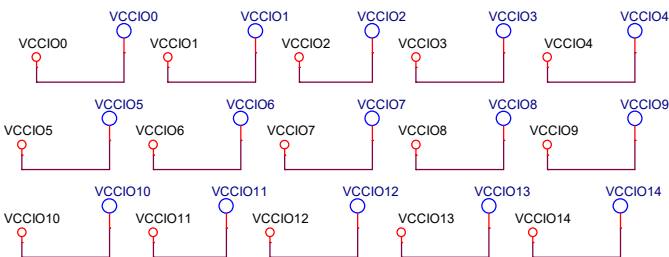
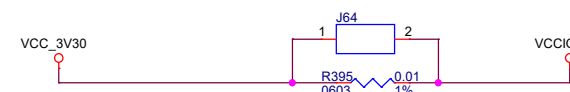
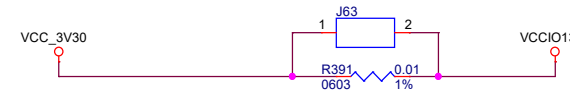
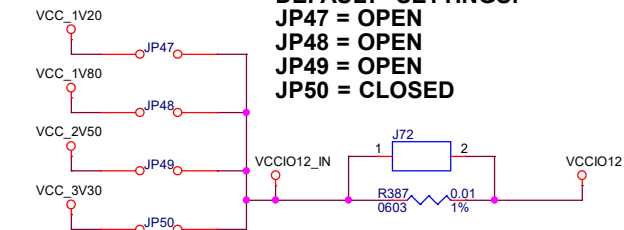
DEFAULT SETTINGS:
JP61 = OPEN
JP75 = CLOSED
JP76 = OPEN



DEFAULT SETTINGS:
JP62 = OPEN
JP77 = CLOSED
JP78 = OPEN

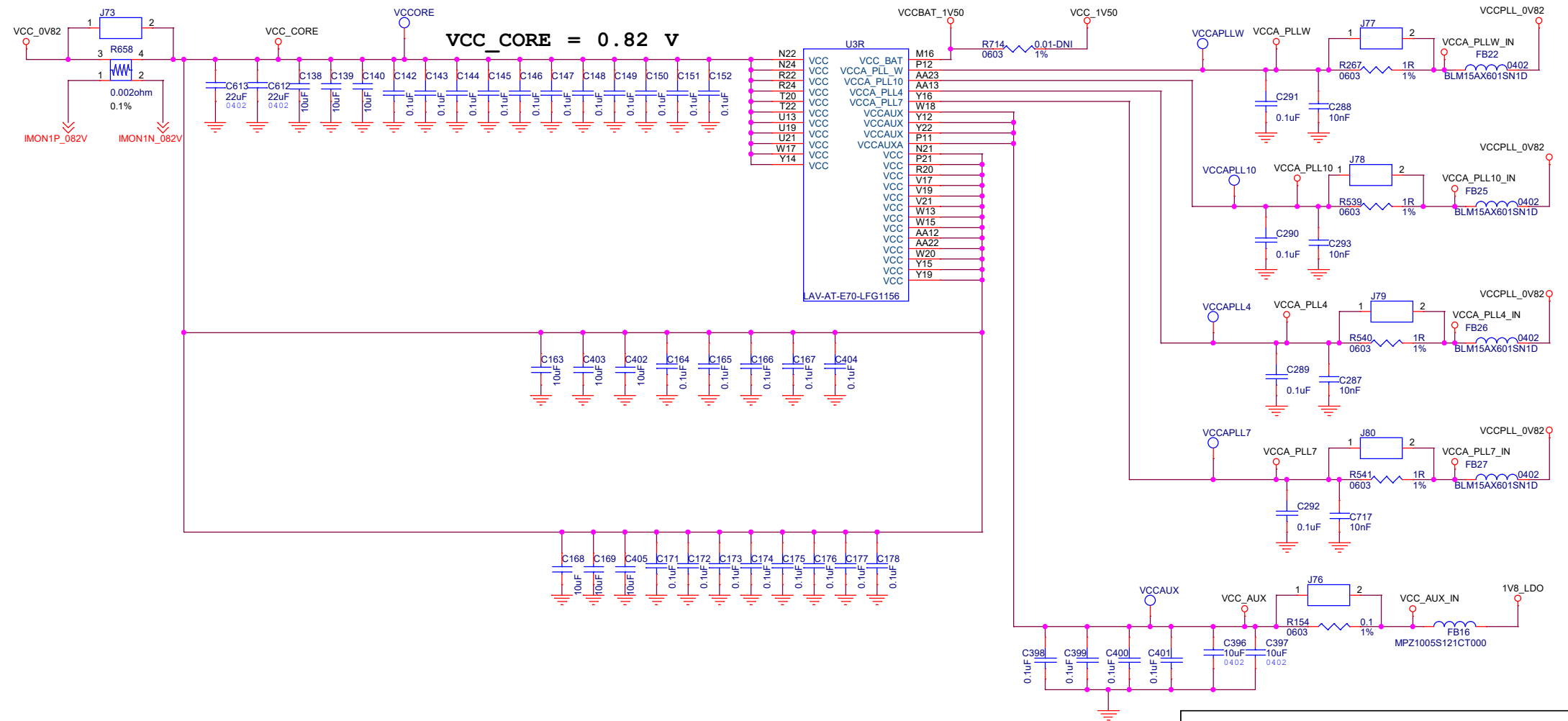


DEFAULT SETTINGS:
JP47 = OPEN
JP48 = OPEN
JP49 = OPEN
JP50 = CLOSED



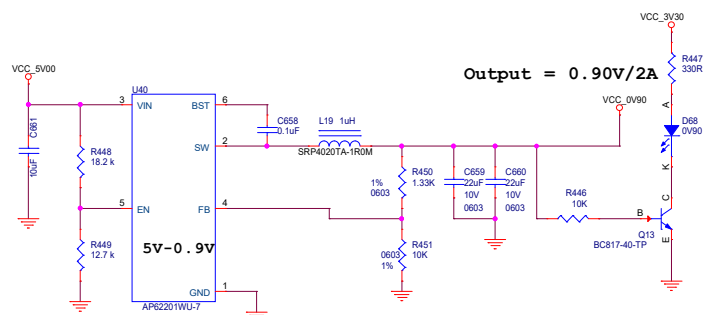
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Title Bank Power		
Size B	Project Avant-E70 Development Board	Schematic Rev 1.0
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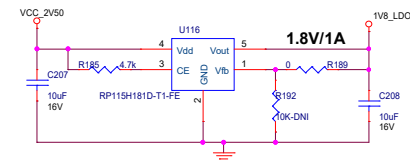
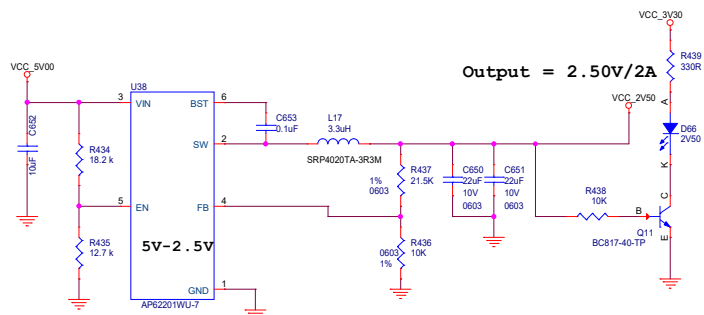
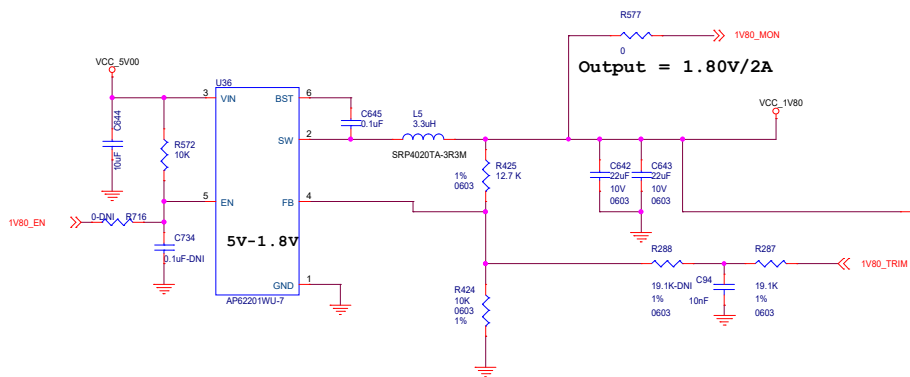
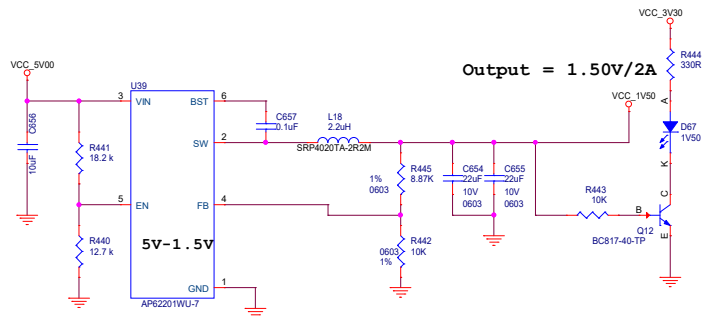
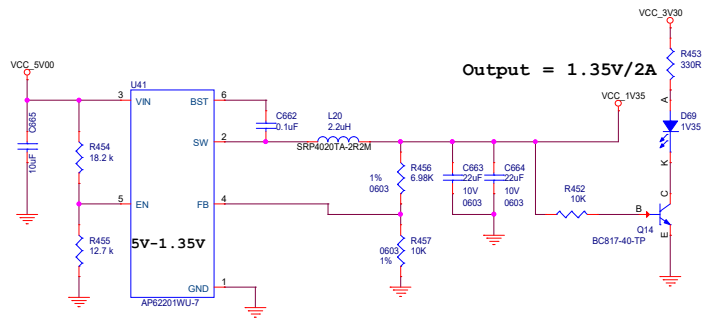
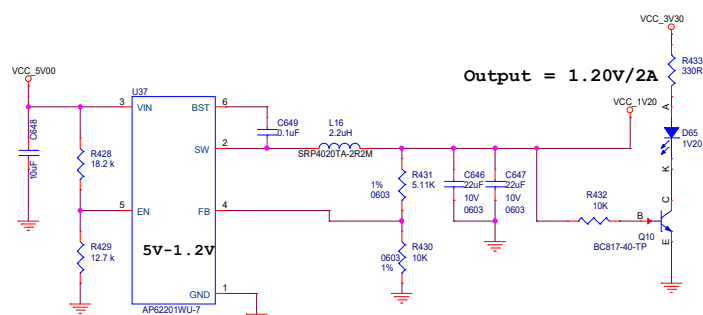
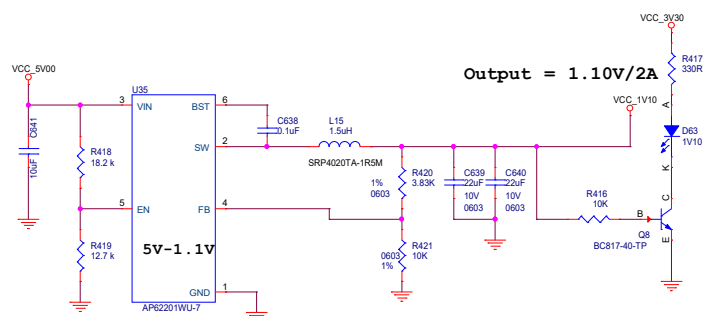
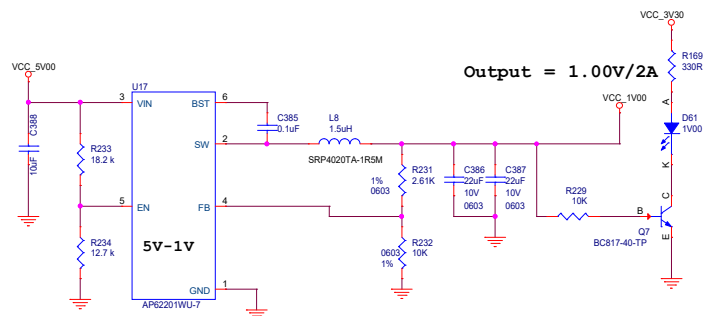


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Title		
Power Decoupling		
Size B	Project	Schematic Rev 1.0
	Avant-E70 Development Board	Board Rev A
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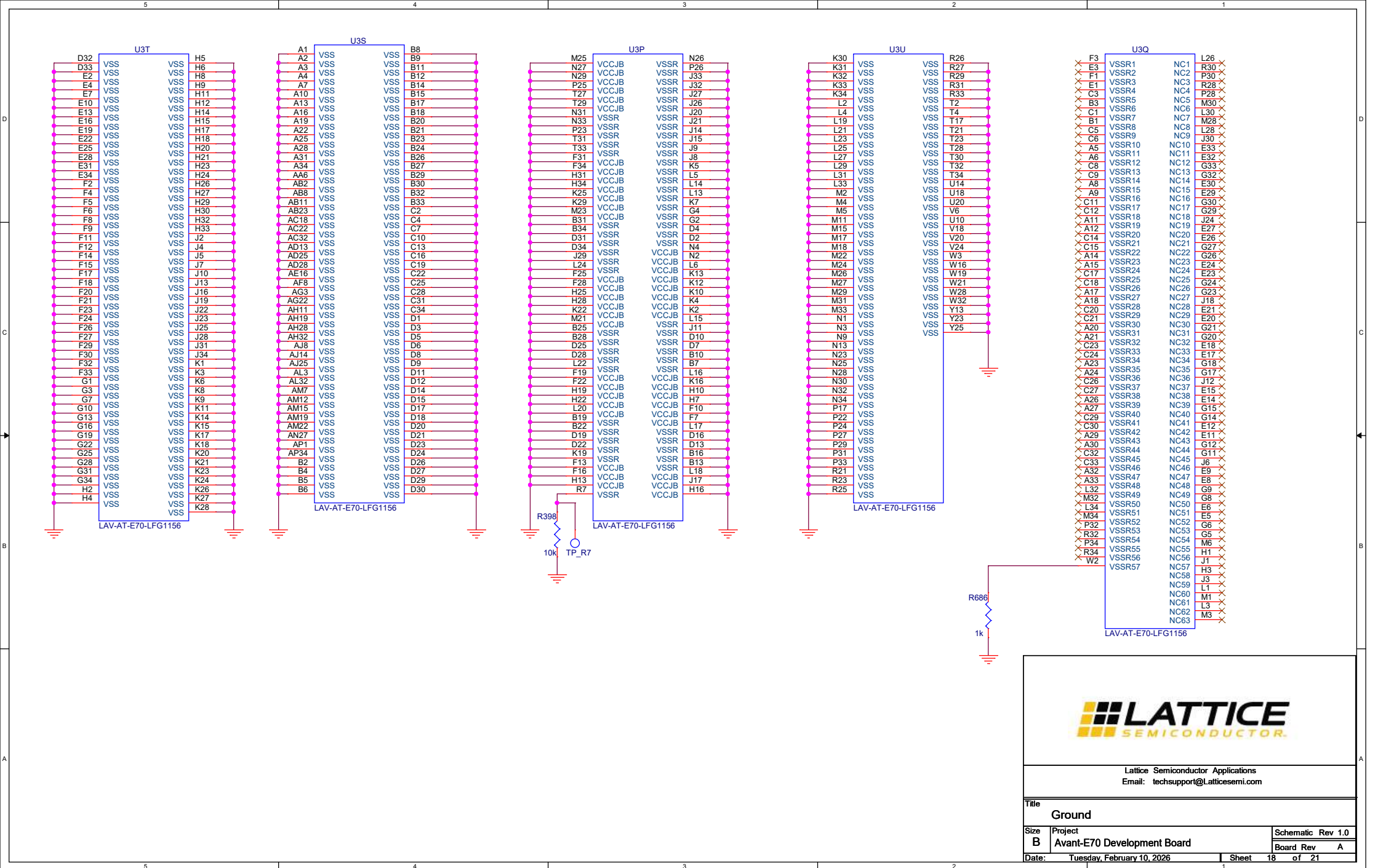


$$V_{\text{output}} = ((R450/R451)+1) \cdot 0.8$$



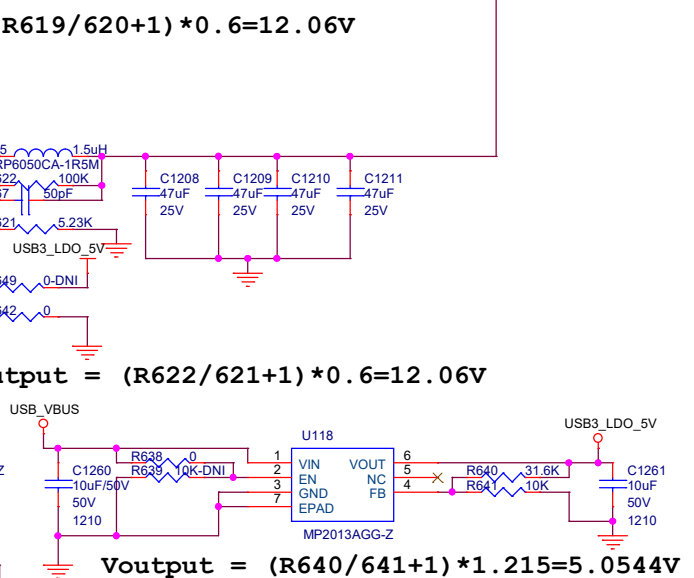
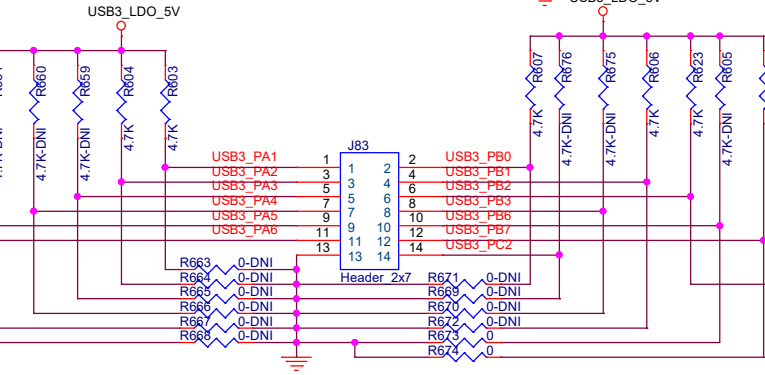
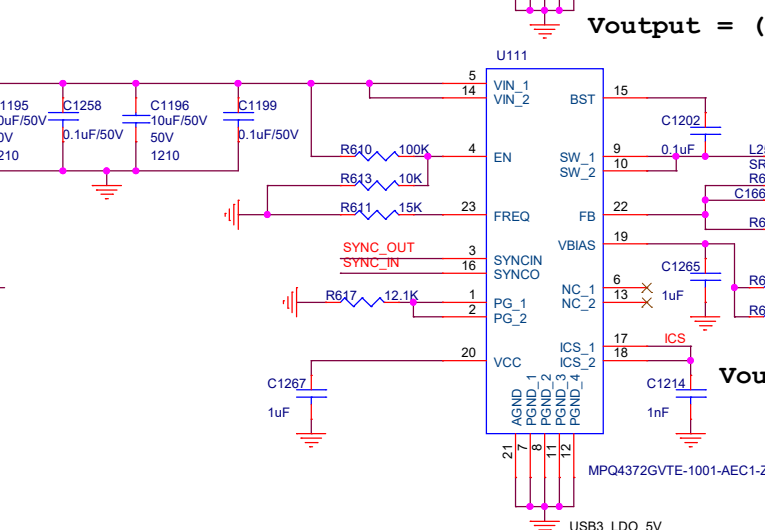
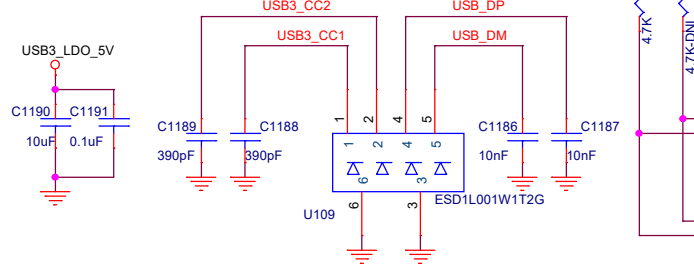
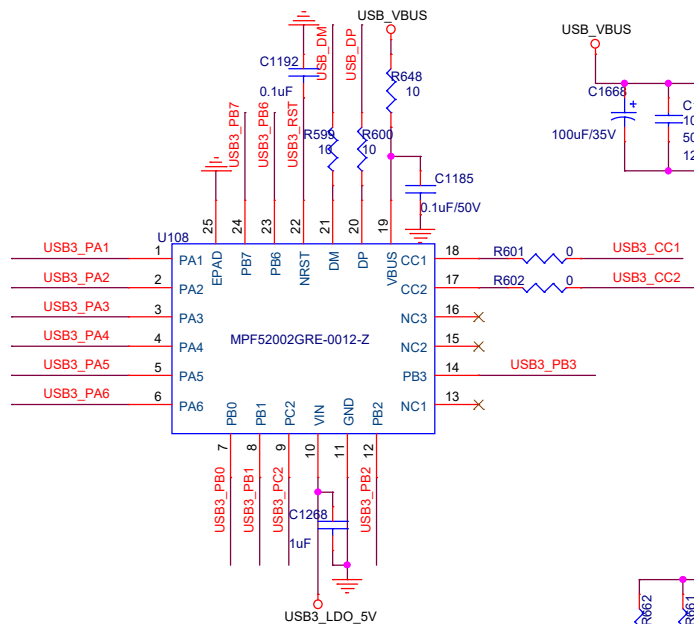
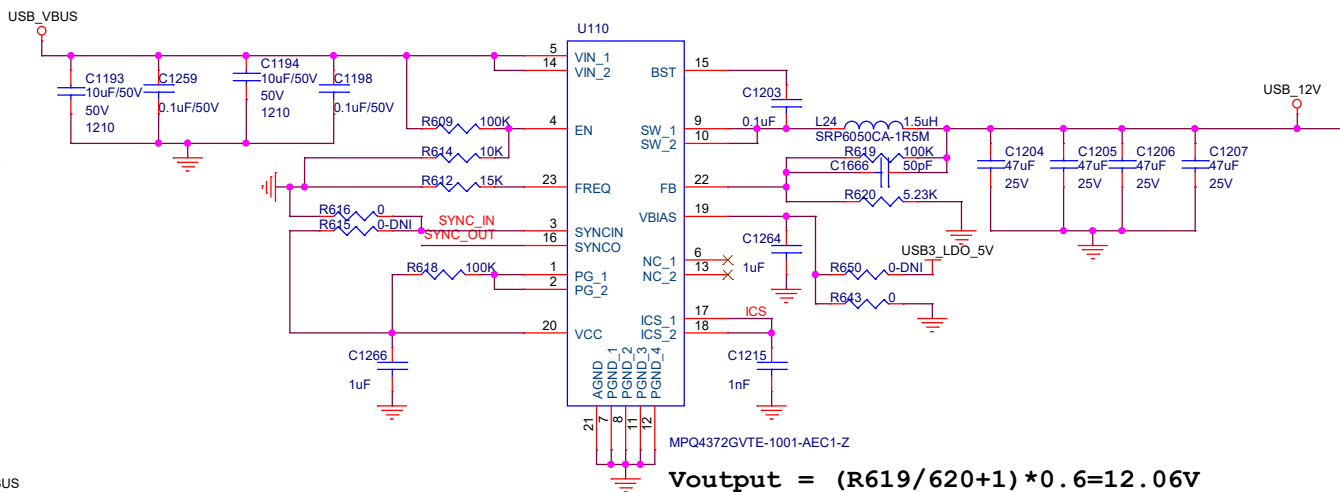
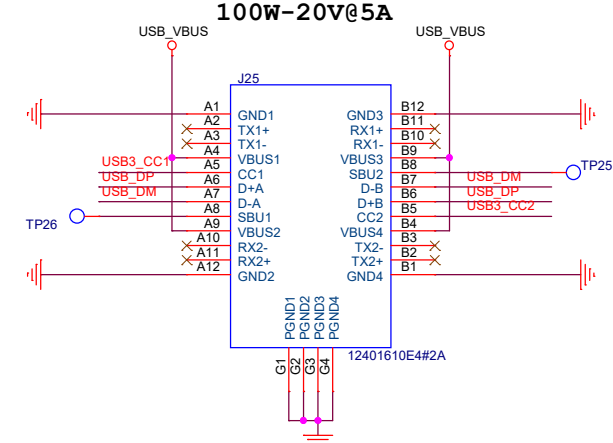
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Title Power Supplies 1		
Size C	Project Avant-E70 Development Board	Schematic Rev 1.0
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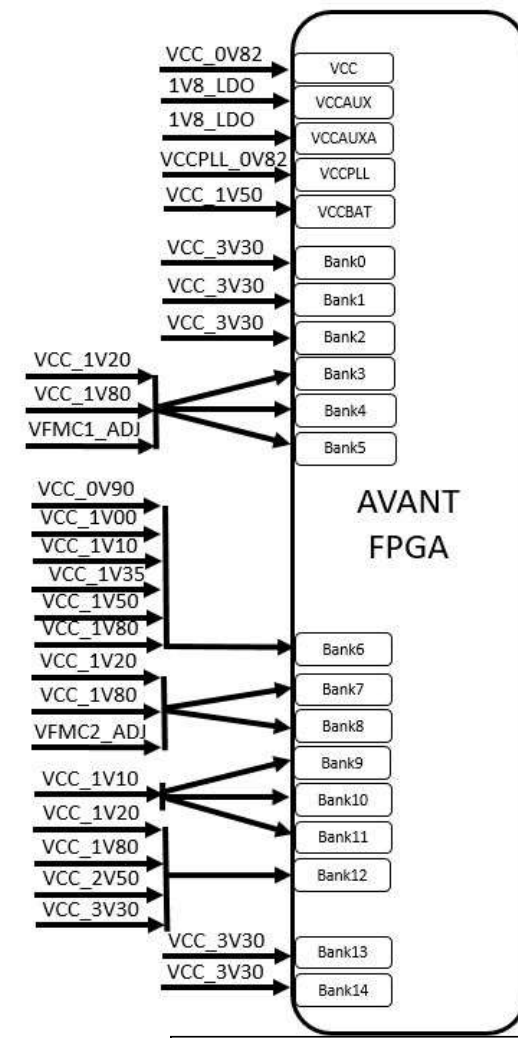
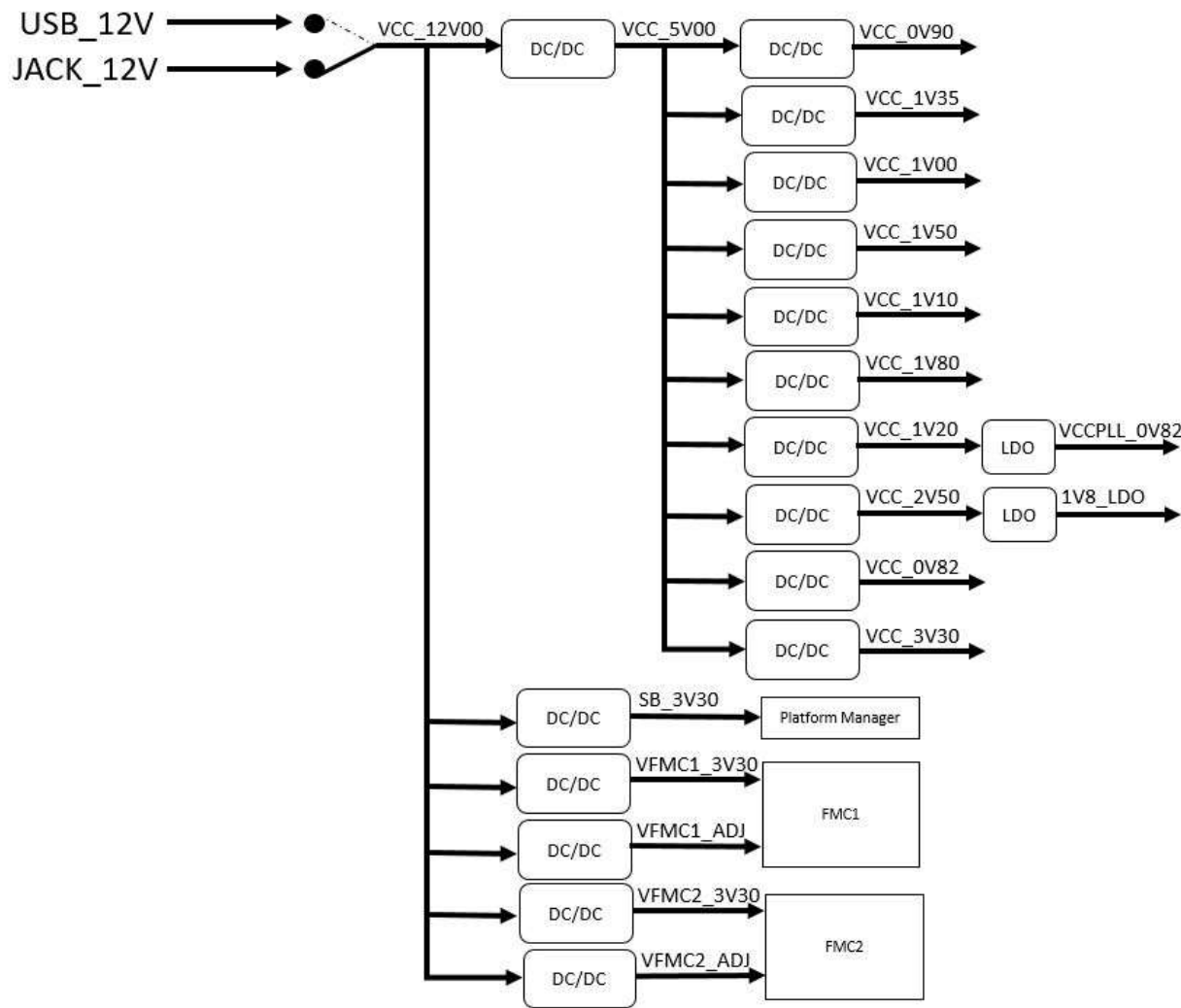


100W-20V@5A



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Title		
USB Power Sink		
Size	Project	Schematic Rev 1.0
B	Avant-E70 Development Board	Board Rev A
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Title		
Power Block Diagram		
Size	Project	Schematic Rev 1.0
B	Avant-E70 Development Board	Board Rev A
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